PURIFI

PURE SOUND

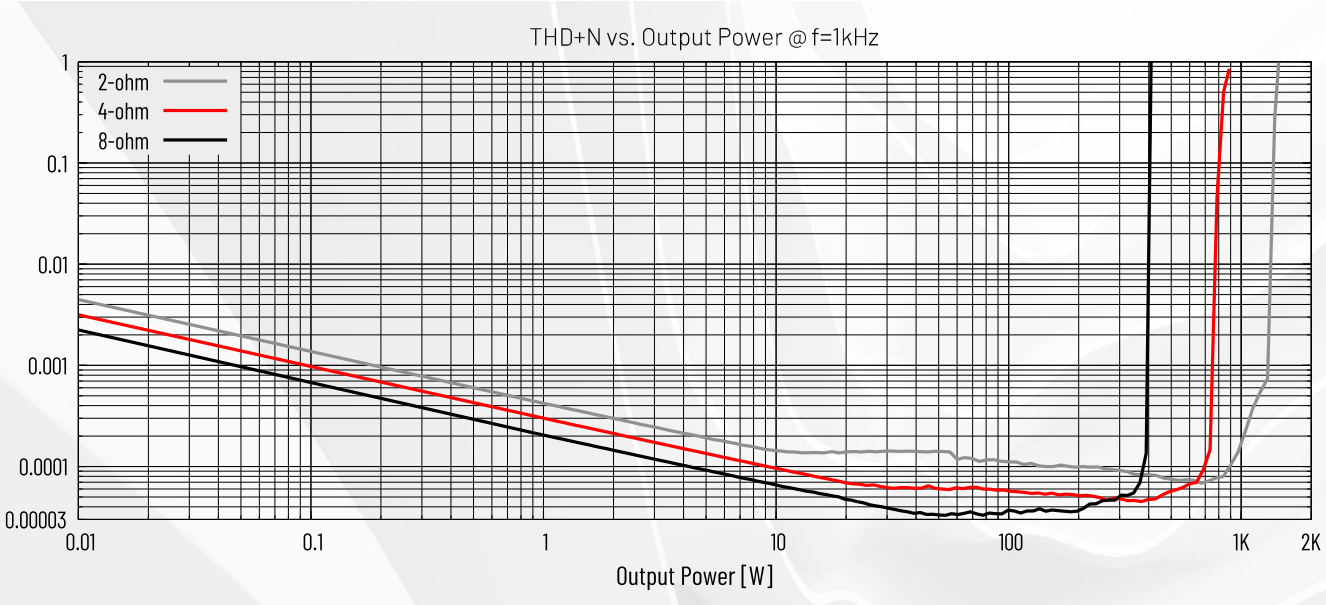
Building a Straight Wire to the Soul of Music

1ET9040BA
DATA SHEET

- 2nd Generation EIGENTAKT Analog-input Class D Amplifier
- Bridged Output Stage
- Negligible THD and IMD
- Extraordinarily Low Noise
- Load-invariant Response
- Exceptionally Clean Clipping
- Low Losses & High Efficiency

KEY SPECIFICATIONS

Output Power @ 0.1% THD	375W @ 8Ω
	750W @ 4Ω
	1400W @ 2Ω
THD+N	<0.00006% @ 100W, 4Ω, 1kHz
Dynamic Range	140dB(A)
Output Noise	4.5μV(A)
Gain	14.4dB
Efficiency	96% @ 1kHz, 750W, 4Ω
Output Current	40A
Supply	±30V to ±45V DC
Size	100mm(width) x 100mm(length) x 35mm (height)



1 Specifications

1.1 Absolute Maximum Ratings

Referenced to GND unless otherwise noted.

Parameter		Min	Max	Unit
Power Supplies	Power Stage Supply, positive rail voltage (+VP)	-0.3	50	V
	Power Stage Supply, negative rail voltage (-VP)	-50	0.3	V
	Gate Drive Supply, voltage, referenced to -VP (VDR)	-0.3	20	V
	OPAMPs supply, positive rail voltage (+VOP)	-0.3	16.5	V
	OPAMPs supply, negative rail voltage (-VOP)	-16.5	0.3	V
	Digital Supply, voltage (+5D, +5A) (optional use)	-0.3	6	V
I/O's	Analog Inputs (+AIN, -AIN)	-20	20	V
	Logic-level outputs, continuous current (SMPS_OFF, GPIO/INT, ICL, VCL)		10	mA
	Logic-level inputs, voltage (/AMPON, SDA, SCL, /FATAL)	-0.3	4.2V	V
	Open-drain, bi-directional, continuous current (SDA)		10	mA
Env.	Ambient temperature	0	100	°C
	Heatsink temperature	0	100	°C
	Relative Humidity, non-condensing		85	%

Stress beyond Absolute Maximum Ratings may cause permanent damage to 1ET9040BA and associated circuitry. Attempts to operate 1ET9040BA within Absolute Maximum Rating but outside Recommended Operation Conditions may result in non-functional circuits and erroneous behavior.

Table 1 Absolute Maximum Ratings

1.2 Recommended Operating Conditions

Amplifier operation is permitted only under conditions stated in Table 2.
Referenced to GND unless otherwise noted.

Parameter		Min	Typ[1)]	Max	Unit
Power Supplies					
+VP	Power Stage, positive rail voltage	30	45	48	V
-VP	Power Stage, negative rail voltage	-48	-45	-30	V
VDR	Gate Drive, voltage (must be referenced to -VP)	13.6	15	17.5	V
+VOP	OPAMPs, positive rail voltage	11.4	12	16	V
-VOP	OPAMPs, negative rail voltage	-15	-12	-11.4	V
+5D	Digital, voltage input	4.5	5	5.5	V
+5A	Analog, voltage input	4.5	5	5.5	V
I/O's					
V_{in_dif}	Analog Inputs, differential rms voltage (pos. to neg. input) required for typ. rated power		14.2[2)]		V
V_{in_cm}	Analog Inputs, common-mode voltage (DC-only)	-5	0	5	V
R_L	Speaker Load, resistive		2-16		Ω
Z_L	Speaker Load, capacitive		0	0.47	µF
Environmental					
T_A	Ambient temperature (ambient air temperature, free airflow)	0	25	75	°C
T_{HS}	Heatsink temperature	0	25	75	°C
θ_{HS-A}	Thermal resistance, Heatsink to Ambient		see note[3)]		°C/W
RH	Humidity, relative (non-condensing)		50	85	%

1) The amplifier is operational within the min-to-max range; audio performance specs may vary outside of Typical (Typ) operating conditions.
2) Corresponds to approximately full Typ rated power in 4Ω load condition.
3) The required θ_{HS-A} depends highly on the desired sustained power delivery specification.

Table 2 Recommended Operating Conditions

1.3 Audio Characteristics

R_L=4Ω, T_A=25° free operating air, f=1kHz, 20kHz AES17 filter (AP), typical operating conditions unless otherwise noted.

Parameter		Conditions	Min	Typ[1)]	Max	Unit
P_O	Output Power, Short term[1)]	R_L= 8Ω, 0.1%THD		375		W
		R_L= 4Ω, 0.1%THD		750		W
		R_L= 2Ω, 0.1%THD		1400		W
	Output Power, Continuous	-		(as limited by thermal system)		-
THD+N	Total Harmonic Distortion + Noise	P_O=1W, f=1kHz		0.0003		%
		P_O=10W, f=1kHz		0.0001		%
		P_O=100W, f=1kHz		0.00006		%
		P_O=400W, f=1kHz		0.000045		%
		P_O=1W, f=20-20kHz		0.0003		%
		P_O=10W, f=20-20kHz		0.0001		%
		P_O=100W, f=20-20kHz		0.00015		%
		P_O=400W, f=20-20kHz		0.0001		%
IMD	Intermodulation Distortion, CCIF	P_O=1W, f=18.5kHz+19.5kHz		0.0001		%
		P_O=10W, f=18.5kHz+19.5kHz		0.0001		%
		P_O=200W, f=18.5kHz+19.5kHz		0.0001		%
ICN	Idle Noise, speaker output	R_L= 4Ω, A-weighted		4.5		µV
DNR	Dynamic Range	A-weighted, rel. to short term P_O, R_L= 4Ω		140		dB
SNR	Signal to Noise Ratio	A-weighted, rel. to short term P_O, R_L= 4Ω		140		dB
BW	Frequency Response, lower -3±½dB	R_L= ∞Ω, V_o=2.83V@1kHz		(DC coupled)		-
		R_L= 8Ω, V_o=2.83V@1kHz (=1W)				
		R_L=4Ω, V_o=2.83V@1kHz				
		R_L= 2Ω, V_o=2.83V@1kHz				
	Frequency Response, upper -3±½dB	R_L= ∞Ω, V_o=2.83V@1kHz		65		kHz
		R_L= 8Ω, V_o=2.83V@1kHz (=1W)		65		kHz
		R_L=4Ω, V_o=2.83V@1kHz		65		kHz
		R_L= 2Ω, V_o=2.83V@1kHz		65		kHz
RESP	Frequency Response, flatness	R_L= ∞Ω, f= 20-20kHz		0.02		dB
		R_L= 8Ω, f= 20-20kHz		0.02		dB
		R_L= 4Ω, f= 20-20kHz		0.02		dB
		R_L= 2Ω, f= 20-20kHz		0.02		dB
Z_O	Output Impedance[2)]	1kHz, I_{out}=1A		0.025		mΩ
		20-20kHz, I_{out}=1A		<0.2		mΩ

1) Assumes a thermal system of adequate size to keep the amplifier module well within its thermal recommended operating range.
2) The Output Impedance is measured with kelvin connection right on the speaker terminal pads (right after the LC filter).

Table 3 Audio Characteristics

1.4 Typical Audio Performance, Graphs

T_A=25° free operating air, 20kHz AES17 filter (AP), typical operating conditions (Table 2) unless otherwise noted.

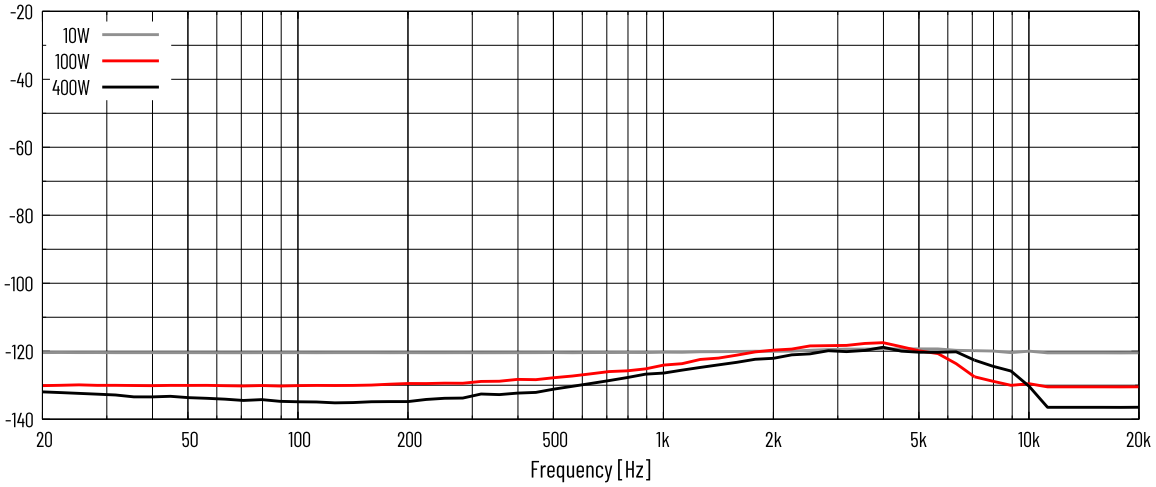


Figure 1 THD [dB] vs. Frequency @ 4Ω

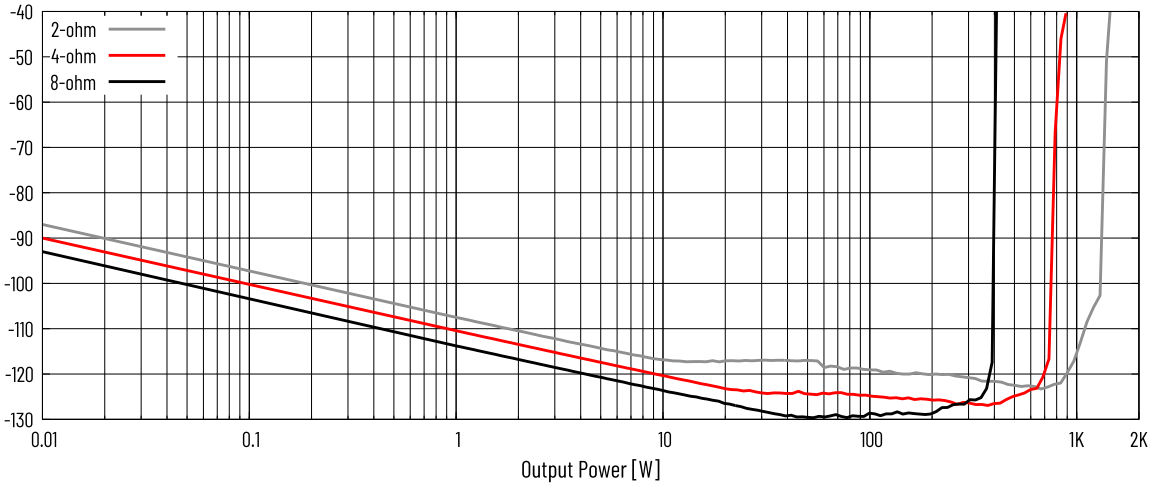


Figure 2 THD+N [dB] vs. Power @ f=1kHz

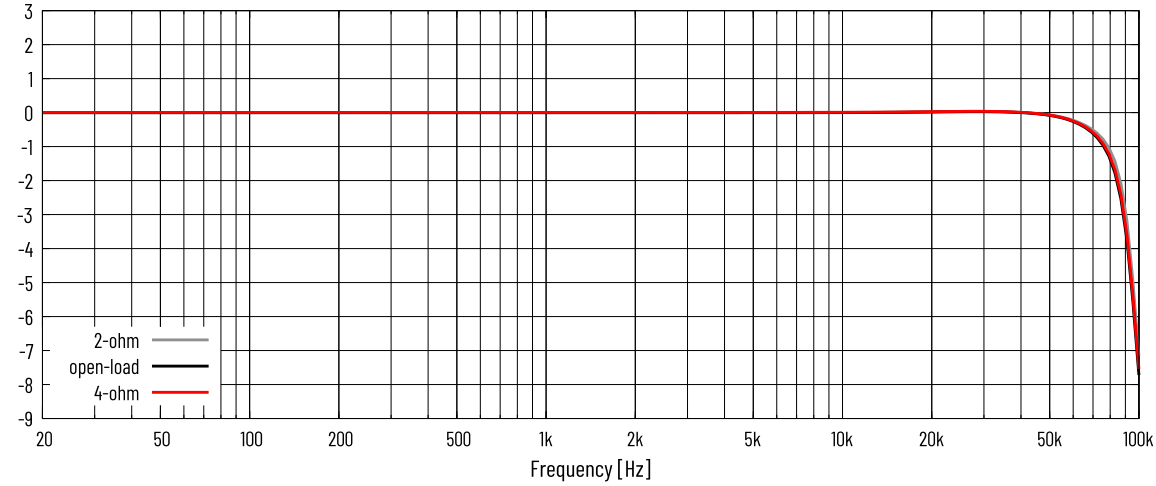


Figure 3 Frequency Response[1] @ V_i=2.83V

1) No AES 17 filter

T_A=25° free operating air, typical operating conditions (Table 2) unless otherwise noted.

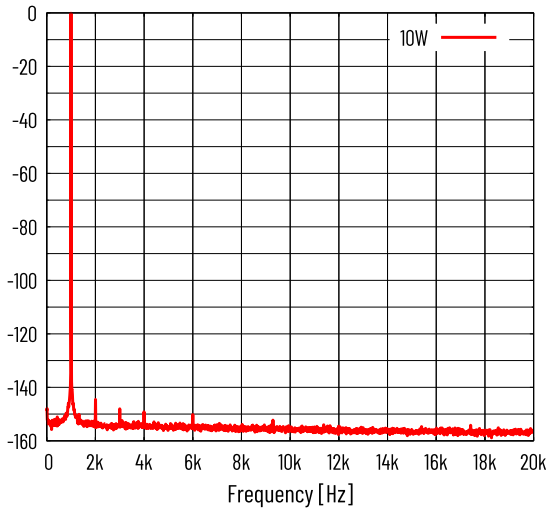


Figure 4 Frequency Spectrum (FFT) @ 1kHz, 10W, 4Ω

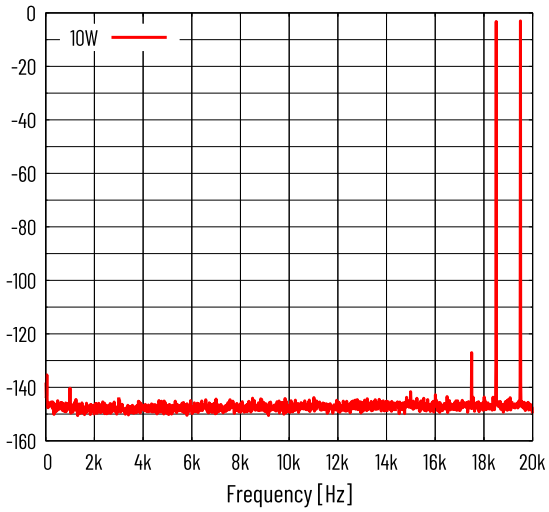


Figure 5 IMD @ 18.5+19.5kHz, 10W, 4Ω

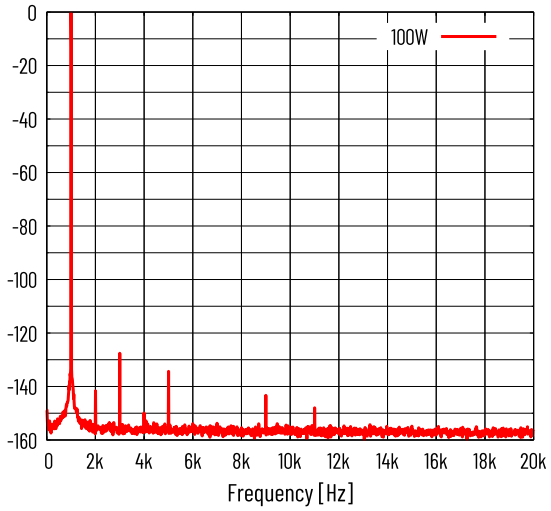


Figure 6 Frequency Spectrum (FFT) @ 1kHz, 100W, 4Ω

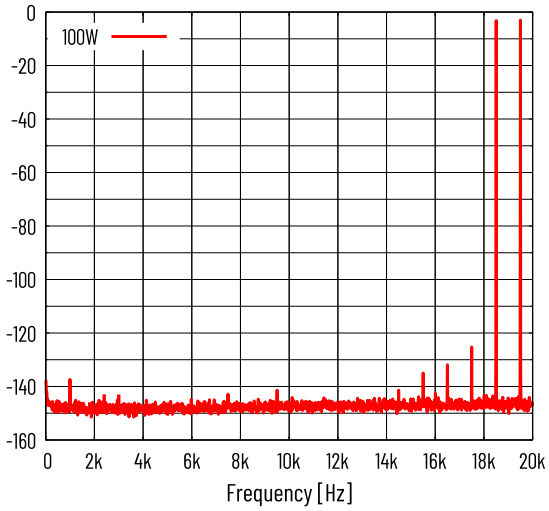


Figure 7 IMD @ 18.5+19.5kHz, 100W, 4Ω

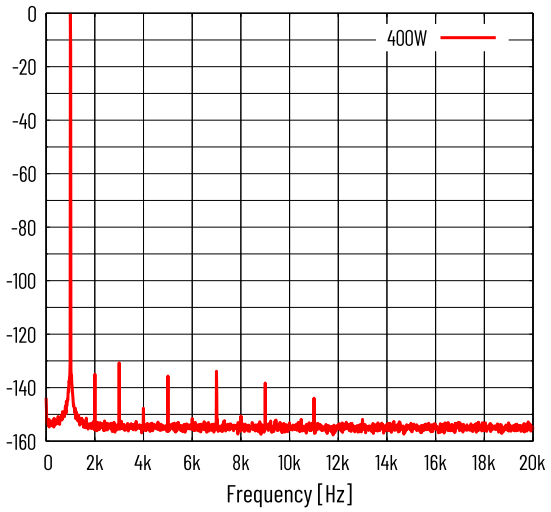


Figure 8 Frequency Spectrum (FFT) @ 1kHz, 400W, 4Ω

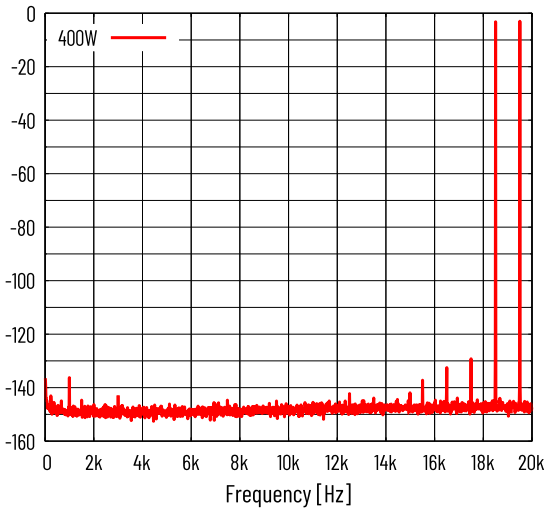


Figure 9 IMD @ 18.5+19.5kHz, 400W, 4Ω

Note: Noise floor dominated by measurement equipment (AP)

T_A=25° free operating air, typical operating conditions (Table 2) unless otherwise noted.

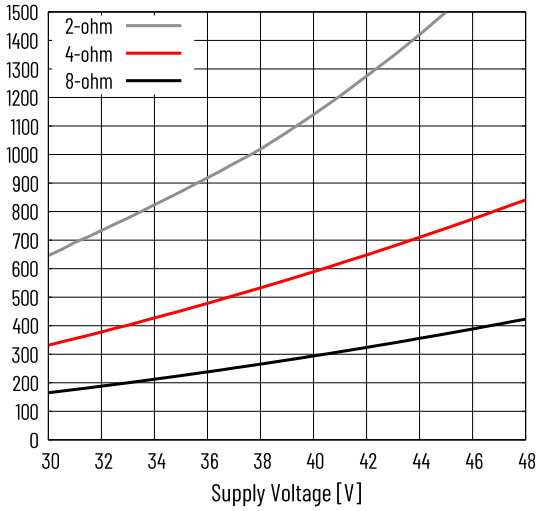


Figure 10 Output Power vs. VP @ 0.1% THD

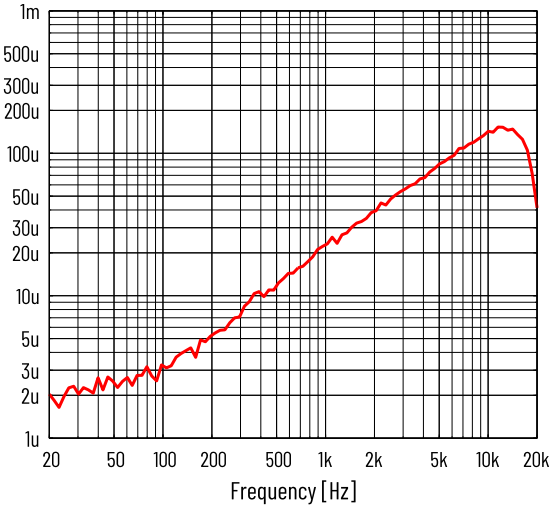


Figure 11 Output Impedance[1] vs. Frequency

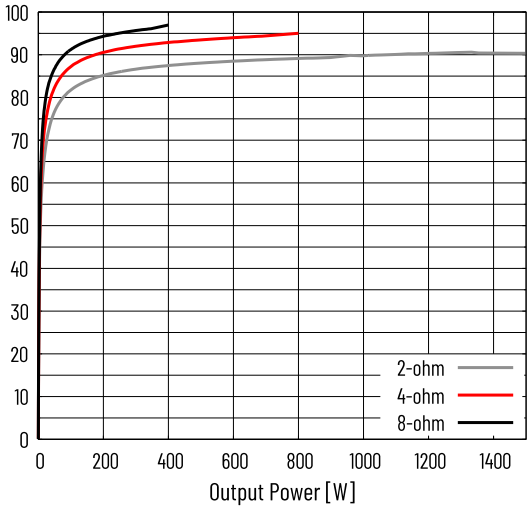


Figure 12 Power Stage Efficiency vs. Output Power

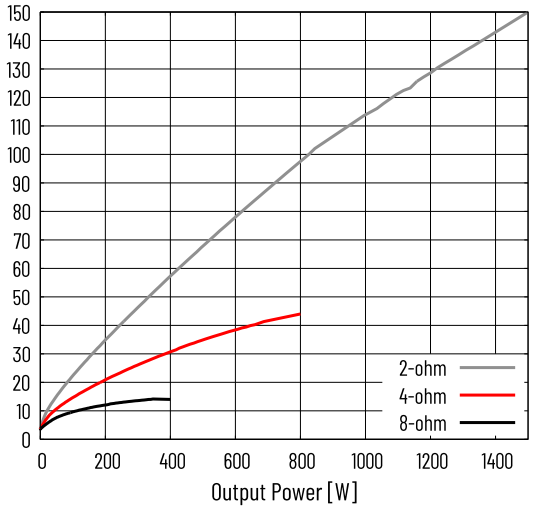


Figure 13 Power Stage Loss vs. Output Power

1) Output impedance is measured using 4-terminal connection. The test current is injected into the +/- terminal pair of J2, the resulting voltage measured back via the remaining terminal pair.

1.5 Electrical Characteristics

R_L=4Ω, T_A=25° free operating air, f=1kHz, 20kHz AES17 filter (AP), typical operating conditions unless otherwise noted.

Parameter		Conditions			Min	Typ	Max	Unit
Current Consumption & Efficiency								
$\lvert I_{VP} \rvert$	Power Stage supply, current	(+VP,-VP), Idle				43		mA
I_{DR}	Gate Drive supply, current	(VDR), Normal operation				60		mA
$\lvert I_{OP} \rvert$	OPAMPs supply, current	(+VOP, -VOP), Normal operation				34		mA
I_{VD}	uC and logic supply, current	(VD), Normal operation				16		mA
I_{VA}	Comparator/analog path supply, current	(VA), Normal operation				8		mA
η	Efficiency, full rated power	R_L= 8Ω				97		%
		R_L= 4Ω				96		%
		R_L= 2Ω				92		%
Audio Inputs & Output								
R_{in}	Input impedance	Differential, pos. to neg. input				1.5		kΩ
		Single-ended, input to GND				1.3		kΩ
A_V	Voltage Gain	V_o/V_i				14.4		dB
$V_{in\_01\%THD}$	Differential, or Single-ended input voltage	To get 0.1%THD @ R_L= 4Ω, VP=±45V				10.5		V_{rms}
$V_{in\_1\%THD}$		To get 1%THD @ R_L= 4Ω, VP=±45V				11.0		V_{rms}
CMRR	Common Mode Rejection Ratio	Audio input, 1kHz				>50		dB
PSRR	Power Supply Rejection Ratio	Forced 1Vrms f≤1kHz ripple, either rail				>90		dB
$\lvert V_{o\_DC} \rvert$	Speaker Output, DC offset	R_L= 4Ω, Grounded analog inputs				<10		mV
f_s	Switching frequency	Idle (indicative)				620		kHz
		Positive clipping				>50		kHz
		Negative clipping				0		Hz
-	Switching residual on output (ripple)	R_L= ∞Ω, Grounded analog inputs				0.25		V_{rms}
Logic Control Signals								
V_{IH}	High level input threshold	(/ENABLE)			2.7			V
V_{IL}	Low level input threshold						0.65	V
V_{IH_I2C}	High level input threshold	(SDA)			2.3			V
V_{IL_I2C}	Low level input threshold						1	V
V_{OH_I2C}	High level output voltage	(SDA)	Open-drain	I=6mA	2.6			V
V_{OL_I2C}	Low level output voltage			I=10mA			0.6	V
I_{OL_I2C}	Low level sink current						10	mA
V_{IH_SCL}	Open collector input	(SCL)			1.65			V
V_{IL_SCL}							0.5	
I_{IH_SCL}							0.001	mA
I_{IL_SCL}							1	
I_{OOC}	Open collector output	(/FATAL)					10	mA
V_{OOC}							65	V
V_{OH}	High level output voltage	(READY, ICL, VCL, GPIO/INT)			VD-0.7			V
V_{OL}	Low level output voltage						0.6	V

Table 4 Electrical Characteristics

Electrical Characterization, continued

R_L=4Ω, T_A=25° free operating air, f=1kHz, 20kHz AES17 filter (AP), typical operating conditions unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Protection Systems						
I_{OCP}	Overcurrent Protection, nominal threshold at normal operation	R_L= 1Ω, f= one pulse 1kHz		40		A
	Overcurrent Protection, nominal derated threshold at high temp	R_L= 1Ω, f= one pulse 1kHz ,VP=OVP$_{VP}$, Temp=OTE		25		A
I_{OCP_VP}	Overcurrent Protection Voltage threshold			45		V
	Overcurrent Protection Voltage rate	I_{OCP} reduction for VP above I_{OCP_VP}		2		A/V
I_{OCP_T}	Overcurrent Protection temperature threshold for deration of OC limit			50		°C
	Overcurrent Protection Voltage rate	I_{OCP} reduction for Temp above I_{OCP_T}		0.5		A/°C
f_{DCP}	DC Protection, Speaker terminal	Detection filter corner frequency		2.5		Hz
$\lvert V_{DCP}\rvert$		Voltage limit, low-pass filtered signal		12		V
T_{OTP_HS}	Thermal Protection, Heatsink	Over-temperature, 2°C hysteresis		75		°C
T_{UTP_HS}		Under-temperature, 2°C hysteresis		0		°C
T_{OTP_RM}	Thermal Protection, Output Inductors	Over-temperature, 2°C hysteresis		85		°C
T_{UTP_RM}		Under-temperature, 2°C hysteresis		0		°C
$\lvert OVP_{VP}\rvert$	Overvoltage Protection, threshold	(+VP, -VP), 1V hysteresis		|50|		V
OVP_{DR}		(VDR), 0.5V hysteresis		17.5		V
$\lvert OVP_{OP}\rvert$		(+VOP, -VOP) , 0.5V hysteresis		|16|		V
$\lvert UVP_{VP}\rvert$	Undervoltage Protection, threshold	(+VP, -VP) , 1V hysteresis		20		V
UVP_{DR}		(VDR) , 0.5V hysteresis		12.5		V
$\lvert UVP_{OP}\rvert$		(+VOP, -VOP) , 0.5V hysteresis		10.5		V

Table 5 Electrical Characteristics

1.6 Timing Characteristics

Typical operating conditions unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Control Signals						
/AMPON	Mute time	Pin asserted high to Amp output HiZ		300		µs
	Un-mute time	Pin asserted low to Amp output LoZ		300		µs
/FATAL	Amplifier failure to signal assertion	Failure to /FATAL low		10		µs
HS/ADDR	Mode Selection	Power-up to Mode latched		40		µs
GPIO	General Purpose I/O pin	(flexible use)		20		µs
Protection Systems						
U/OVP	Under-/overvoltage protection recovery	From voltage good to Amp output LoZ		20		µs
OLP	Overload Protection, threshold	Ratio of OCP cycles to non-OCP cycles		12		%
t_{OLP}	OLP Mute cycle duration	OLP even to reenable outputs		1		s
t_{DCP}	DCP Mute cycle duration	DCP even to reenable outputs		1		s

Table 6 Timing Characteristics

1.7 Mechanical & Mounting

Parameter		Conditions	Min	Typ	Max	Unit
	Length			100		
	Width			100		mm
	Height			35		mm
Mounting	Threaded standoff	Diameter		M3		-
		Available thread depth			4	mm
		Torque[1)]			0.5	Nm

1) Observe torque spec for the selected standoff/screw/nut.

Table 7 Mechanical & Mounting

1.8 Overview

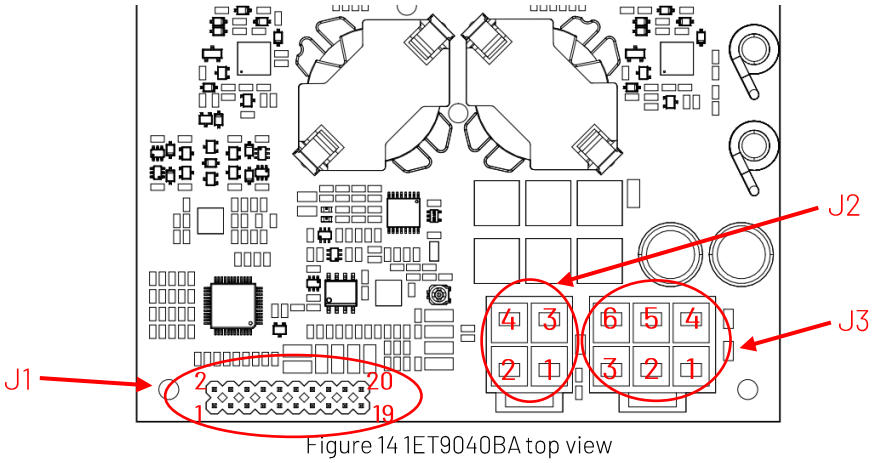


Figure 14 1ET9040BA top view

Node	Signal	Rating	I/O	Description
J1				
J1:1	GND	Table 1 Table 2	-	Common ground for all circuits
J1: 2	+5D		P	External Voltage supply logic-level circuits
J1: 3	READY		O	Amplifier "Ready" – signal goes low on error
J1: 4	/ENABLE		I	Amplifier Enable (HW Mode) – *pull low to enable Amp*
J1: 5	ICL		O	Output Current clipping
J1: 6	VCL		O	Output Voltage clipping
J1: 7	ADDR		I	HW/SW Mode/I2C Address Selection; set by one 1% resistor.
J1: 8	GPIO/INT[1)]		X	General Purpose I/O pin; function depends on Register map configuration
J1: 9	SDA		X	I2C Data (SW Mode)
J1: 10	SCL		I	I2C clock (SW Mode)
J1: 11	/FATAL		O	Amplifier "error/fail" (HW Mode) – signal goes low on error
J1: 12	+5A		P	External Voltage supply analog low-voltage circuits
J1: 13	GND		-	Common ground for all circuits
J1: 14	GND		-	Common ground for all circuits
J1: 15	IN+		I	Analog Input, positive
J1: 16	IN-		I	Analog Input, negative
J1: 17	GND		-	Common ground for all circuits
J1: 18	GND		-	Common ground for all circuits
J1: 19	+VOP		P	OPAMPs, positive rail
J1: 20	-VOP		P	OPAMPs, negative rail
J2				
J2: 1	OUT+	2.3.2	O	Speaker Output, positive
J2: 2	OUT-		O	Speaker Output, negative
J2: 3	OUT+		O	Speaker Output, positive
J2: 4	OUT-		O	Speaker Output, negative
J3				
J3: 1	VDR	Table 1 Table 2	P	Gate Drive Supply, referenced to -VP
J3: 2	+VP		P	Power Stage Supply, positive rail
J3: 3	GND		-	Common ground for all circuits
J3: 4	-VP		P	Power Stage Supply, negative rail
J3: 5	-VP		P	Power Stage Supply, negative rail
J3: 6	GND		-	Common ground for all circuits

1)GPIO pin can used to pull an interrupt on the system uC where after the protection status can be read via I2C.

Table 8 I/O

Connector	Equivalent Type	Matching cable part
J1	Würth 61302021121	IDC-20 Female
J2	JST: B04P-VL	JST: VLP-04V
J3	JST: B06P-VL	JST: VLP-06V

Table 9 I/O Connector Types

2 Configuration Requirements & System Considerations

2.1 Power Supplies

Voltage, current and power ratings are described in detail in Table 2 Recommended Operating Conditions and Table 4 Electrical Characteristics.

2.1.1 Power Stage Supply (+VP, -VP)

1ET9040BA requires a ground-centered (GND) split-rail supply for the amplifier output stage.

2.1.2 Gate Drive Supply (VDR)

The design requires an external supply for the gate drive circuitry. It is essential that the supply is designed as a floating rail, that must be referenced to -VP. VDR directly feeds the low-side gate driver; the amplifier utilizes boot-strap circuitry to create a rail relative to the high-side driver.

2.1.3 OPAMPs Supply (+VOP, -VOP)

1ET9040BA requires an external ground-centered split-rail supply for the op-amp circuitry.

2.1.4 Low power circuitry supply (+5A, +5D)

1ET9040BA requires an external supply for digital and low power analog circuitry.

2.2 Control Signals

2.2.1 SDA

SDA is used in SW mode and is a bi-directional I/O and complies with the general I2C specification in terms of levels and timing.

SDA is tied directly to an onboard microcontroller GPIO pin.

2.2.2 SCL

SCL is used in SW mode and is an input complying with the general I2C specification in terms of levels and timing.

SCL is tied directly to an onboard microcontroller GPIO pin.

2.2.3 /ENABLE

/ENABLE is used in HW mode. The amplifier is enabled when /ENABLE is pulled low (refer to section 4).

/ENABLE is tied directly to an onboard microcontroller GPIO pin.

2.2.4 /FATAL

/FATAL is connected to the collector of a transistor which has the emitter tied to an onboard microcontroller GPIO pin and the base tied permanently to VD via a 3.3kΩ resistor. The pin will pass output from the microcontroller and function as open-collector output.

2.2.5 ADDR

A programming resistor must be connected between the ADDR pin and GND in order to enable SW mode and to set I2C register address. Please refer to Table 10 for resistor values and I2C addresses. HW mode is enabled when ADDR is left open (when the programming resistor is not mounted).

2.2.6 GPIO/INT

General-purpose I/O, may be programmed to signal status changes. Please refer to section 4.2.2 for details.

GPIO/INT is tied directly to a microcontroller GPIO pin.

2.2.7 ICL & VCL

ICL indicates current clipping and is asserted high each time a PWM cycled is terminated early by OC detection. ICL status is updated by the system microcontroller with a delay less than 40µs.

VCL indicates voltage clipping and is asserted high each time voltage clipping is detected. VCL status is updated by the system microcontroller with a delay less than 40µs.

2.3 Audio Inputs & Output

2.3.1 Audio Input (IN+, IN-)

1ET9040BA has a differential analog input.

The behavior of the input can be described as equivalent to a traditional floating differential, op-amp configuration with gain and input resistance as listed in Table 4.

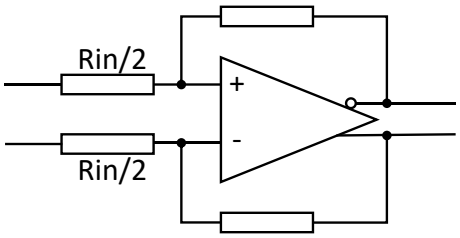


Figure 15 1ET9040BA Equivalent Input Impedance

2.3.2 Speaker Output (OUT+, OUT-)

1ET9040BA has a ground-centered bridge-tied-load (BTL) speaker output.

The output impedance of 1ET9040BA is significantly lower than the resistance of even a single high quality output binding post. To derive the greatest benefit of the ultra-low output impedance, 1ET9040BA is fitted with a four-pole output connector which permits bi-wiring. This prevents load dependent currents from e.g. the bass section of a speaker from impacting the mid/tweeter section. 1ET9040BA's ultra-low output impedance offers a degree of isolation that can otherwise only be matched by full bi-amping.

2.4 Thermal Requirements

While the 1ET9040BA has very low idle losses and high overall efficiency, adequate cooling is essential for sustained power delivery. Careful considerations must be given to the design of the thermal system in order to achieve desired output power specifications. 1ET9040BA's power efficiency and power loss is illustrated in Figure 12 and Figure 13

2.5 Mechanical Requirements

It is the responsibility of the system integrator to ensure integrity of mounting method and materials used. It is recommended to thoroughly test the final product for robustness against, e.g., shock and vibration.

3 Protection System

1ET9040BA is protected from overload and failure by means of several protection circuits. All systems are continuously active while the amplifier is powered and operational.

3.1 Environmental checks

Environmental checks denote circuits that monitor operating conditions maintained or affected by external sources or influences such as power supply voltages and ambient/system temperature.

Environmental checks are enabled in both HW Mode and SW Mode.

3.1.1 Over/Under-Voltage Protection, +VP, -VP, VDR, +VOP, -VOP

The high voltage supply rails (Power Stage Supply), op-amp and gate drive supply rails must be within certain thresholds for safe operation. If supply levels are outside min-to-max thresholds denoted in Table 5 the Amplifier power stage output is brought immediately into high-impedance state (HIZ).

In SW Mode OVP/UVP states are reported in I2C registers.

3.1.2 Temperature Protection

1ET9040BA utilizes circuitry to monitor the temperature of the aluminum back plate (used for cooling the FET's) and take appropriate action if conditions are outside the recommended operating range. A second sensor is placed on the top side of the PCB to monitor the temperature of the two output coils.

An OTP/UTP condition brings the amplifier output into high-impedance state (stop switching). Normal operation automatically resumes once temperatures return within the tolerable range, i.e., no involvement from user or system host controller is required.

In SW Mode OTP/UTP status and actual measured temperature are reported in the I2C register.

3.2 Overcurrent Protection (OCP)

1ET9040BA is protected against short-circuits between speaker output terminals (OUT+ to OUT-), from speaker output terminal to ground. Additionally, the amplifier is protected against extended-time high-current overload situations.

A system monitors the output stage current and abruptly engages a *protection cycle* (*OCP cycle*) if the pre-set overcurrent threshold is exceeded. During a *protection cycle* the output stage reverses state until the following PWM frame. This behavior is comparable to a current-limiter function. Following a *protection cycle*, normal operation is automatically resumed and no involvement from user or system host controller is required.

Short-circuits from speaker output terminal(s) to ground is detected as an error situation and the protection system immediately shuts down the amplifier.

Extended current-limiting will result in triggering of the Overload Protection, OLP.

OCP is enabled in all modes of operation (SW Mode, HW Mode) and reported on ICL.

OCP is reported in the I2C register when operating in SW Mode.

While OVP and OTE protection disables the amplifier when thresholds for voltage and temperature are exceeded, operation at high temperature and VP voltages higher than nominal is still allowed until VP_ OVP, and/or OTE thresholds. Above VP_ OVP and/or above OTE thresholds the OC threshold will decrease as shown in Figure 16.

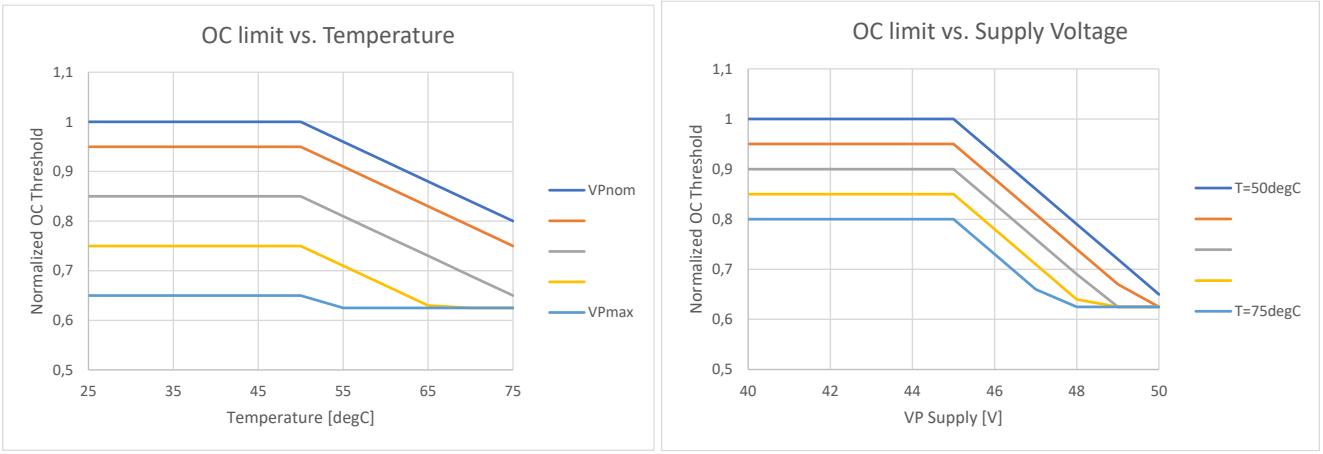


Figure 16 OC Threshold versus Temperature and Supply Voltage

3.3 Overload Protection (OLP)

To safeguard 1ET9040BA against continuous operation at the OCP threshold (i.e., in current limiting) a circuit keeps track of OCP cycles as function of time. If the amplifier is running in current limiting more than approximately 12% over time *an OLP mute cycle* is triggered.

In events of continuous OCP the *OLP mute cycle* triggers after approximately 10ms.

During a *mute cycle* the output stage is disabled (left in high-impedance state) approximately 1 second.

Following a *mute cycle*, normal operation is automatically resumed, i.e., no involvement from user or system host controller is required.

OLP is enabled in all modes of operation (SW Mode, HW Mode).

OLP is reported in the I2C register when operating in SW Mode.

3.4 Output Voltage Clip Protection (CLIP)

To safeguard 1ET9040BA against output voltage clipping, a circuit ensures continuous operation of the power stage high-side boot-strap circuitry by inserting narrow pulses in the output PWM signal.

CLIP is enabled in all modes of operation (SW Mode, HW Mode) and reported on VCL.

CLIP is reported in the I2C register when operating in SW Mode

3.5 DC Protection (DCP)

1ET9040BA is capable of passing DC signals, i.e., the audio channel does not include any form of low-cut (high-pass) filtering.

To protect the speaker against potentially harmful DC signals 1ET9040BA includes a circuit that monitors the speaker output and disables the power stage should certain conditions be exceeded. The speaker output signal is low-pass filtered with a corner frequency below the audible range and if the filtered signal exceeds a pre-set threshold (see Table 5) a DCP *mute cycle* is triggered.

Following a *mute cycle*, normal operation is automatically resumed only if the DC is reduced within safe thresholds. If so, no involvement from user or system host controller is required. However, if DC persists at the end of the *mute cycle*, the power stage is latched off and will stay off until the user or system host controller takes deliberate action to restart operation.

DCP is enabled in SW Mode and HW Mode.

DCP-latch-off condition is reported in the I2C register when operating in SW Mode. Note that a DCP *mute cycle* is not reported.

In HW Mode, DCP-latch-off condition asserts /FATAL signal low. It is recommended that the /FATAL signal is used to switch off the power supplies.

4 Operating Modes & Status Reporting

1ET9040BA can operate in two modes:

1. HW Mode: all control via pins (HW interface)
2. SW Mode: enables I2C control (I2C interface)

Setting of the HS/ADDR signal (by connecting a 1% resistor from HS/ADDR, J1:7, to GND) defines operation mode and I2C address per following table:

Mode	I2C Address	Resistor: ADDR to GND
Hardware Mode	-	∞ (not populated)
Software Mode	0x50	0
	0x51	1K9
	0x52	3K9
	0x53	6K8
	0x54	10K
	0x55	12K
	0x56	18K
	0x57	22K
	0x58	27K
	0x59	33K
	0x5A	47K
	0x5B	56K
	0x5C	82K
	0x5D	120K
	0x5E	190K
	0x5F	390K

*) Resistors must be 1% or better.

Table 10 Mode Selection via HS/ADDR

4.1 HW Mode

In HW mode operation, the protection system controller monitors and operates available circuits for environmental checks (Over/Under-voltage, Temperature) and all protection circuits (Current limiting, Overload protection, DC protection and voltage clipping protection).

In HW Mode, status and control information is accessible via the following signals:

Signal	Rating	I/O	Description
/FATAL	Table 1	O	Amplifier "error/fail" – *signal goes low on error*
/ENABLE		I	Amplifier Enable (HW Mode) – *pull low to enable Amp*
READY		O	Amplifier ready (running, no errors)
ICL		O	Current clip signal. Pulses each time a PWM cycled is terminated early by OC detection.
VCL		O	Voltage clip signal. High during clip

Table 11 Status/Control signals in HW Mode

4.2 SW Mode

In SW mode operation, the channel controller monitors and operates available circuits for environmental checks (Over/Under-voltage, Temperature) and all protection circuits (Current limiting, Overload protection, DC protection and voltage clipping protection).

In SW mode 1ET9040BA can be turned on and off by I2C (see Table 13) when /ENABLE is left unconnected. If /ENABLE is pulled low, 1ET9040BA is enabled.

In SW mode, status and control information is accessible via I2C as well as via several HW signals:

Signal	Rating	I/O	Description
/FATAL	Table 1	O	Amplifier "error/fail" – *signal goes low on error*
/ENABLE		I	Amplifier Enable – *pull low to force enable Amp*
SCL		I	I2C clock
SDA		I	I2C Data
GPIO/INT		O	Interrupt signal, pulls low when any failure flags an error
READY		O	Amplifier ready (running, no errors)
ICL		O	Current clip signal - *pulses high each time a PWM cycled is terminated early by OC detection*
VCL		O	Voltage clip signal. High during clip

Table 12 Status/Control signals in SW Mode

4.2.1 I2C Register Map

Reg	Name	Data type	R/W	Description	
0x00	Channel count	High Nibble	R	1 = module has one active channels	
	Product Type	Low Nibble	R	1 = amplifier module	
0x01 0x02	Model	Integer	R	0x23 0x50	0x2350 = 9040 (dec)
0x03	Version	High Nibble	R	Hardware revision number	
	Revision	Low Nibble	R	Hardware sub-revision number	
0x04 0x05	Serial	Integer	R	Serial number (convert hex to dec to get serial number)	
0x06	Firmware	High Nibble	R	Firmware revision number	
		Low Nibble	R	Firmware sub-revision number	
0x07	Reserved	-	-		
0x08	Reserved	-	-		
0x09	Reserved	Bits 7-4	-		
	GPIOint	Bit 3	W	Set to make GPIO an interrupt pin. In that case, GPIO will go high whenever a non-masked bit in registers 0x0B-0x0D changes, and go low as soon as any of them are read	
	GPIODir	Bit 2	W	GPIO pin direction, 1=input, 0=output	
	GPIOVal	Bit 1	R/W	GPIO pin value	
	AmpEnable	Bit 0	W	Request to turn on amplifier	
0x0A	Reserved	Bits 7-3	-		
	ICLIP	Bit 2	R	Flags that current limiting has happened since this flag was last read	
	VCLIP	Bit 1	R	Flags that at clipping has happened since this flag was last read	
	AmpReady	Bit 0	R	Power stage is switching and passing signal	
0x0B	AmpFail	Bit 7	R	Flags that DC at the output persisted after turning the power stage off	
	OverTemp_Coil	Bit 6	R	Temperature at Coil sensor too high.	
	OverTemp_PS	Bit 5	R	Temperature at FET sensor too high.	
	MinVOPOver	Bit 4	R	Negative op-amp supply too high.	
	PlusVOPOver	Bit 3	R	Positive op-amp supply too high.	
	VDROver	Bit 2	R	VDR too high.	
	MinHVOver	Bit 1	R	Negative high-voltage supply too high.	
	PlusHVOver	Bit 0	R	Positive high-voltage supply too high.	
0x0C	Reserved	Bits 7	-		
	UnderTemp_Coil	Bit 6	R	Temperature at Coil sensor too low.	

Reg	Name	Data type	R/W	Description
	UnderTemp_PS	Bit 5	R	Temperature at Fet sensor too low.
	MinVOPUnder	Bit 4	R	Negative op-amp supply too low.
	PlusVOPUnder	Bit 3	R	Positive op-amp supply too low.
	VDRUnder	Bit 2	R	VDR too low.
	MinHVUnder	Bit 1	R	Negative high-voltage supply too low.
	PlusHVUnder	Bit 0	R	Positive high-voltage supply too low.
0x0D	Reserved	Bits 5-7	-	
	MOSFailError	Bit 4	R	Power stage is turned off after one half stopped responding
	CMError	Bit 3	R	Power stage is temporarily turned off after a common-mode OC event
	Reserved	Bit 2	R	
	OverloadError	Bit 1	R	Power stage is temporarily turned off after a sustained OC event
	DCError	Bit 0	R	Power stage is temporarily turned off after DC detected on the output
0x0E	PlusVP	Unsigned short	R	Measured positive high-voltage rail in volts
0x0F	MinVP	Unsigned short	R	Measured negative high-voltage rail in volts
0x10	VDR	Unsigned short	R	Measured VDR in decivolts.
0x11	Temperature_PS	Signed short	R	Measured temperature at power stage in °C
0x12	Temperature_Coil	Signed short	R	Measured temperature at coil in °C
0x13	DC	Signed short	R	Measured output DC in volts
0x14 0x15	Fsw	Unsigned int	R	Measured switching frequency in units of 250Hz.
0x16	PlusVOP	Unsigned short	R	Measured positive op amp supply, in decivolts
0x17	MinVOP	Unsigned short	R	Measured negative op amp supply, in decivolts
0x18	Reserved	-	-	
	AmpReadyMask	Bit 0	R/W	AmpReady Masking bit (default 0)
	VClipMask	Bit 1	R/W	VClip Masking bit (default 0)
	IClipMask	Bit 2	R/W	IClip Masking bit (default 0)
	Reserved	Bit 3	-	
	Reserved	Bit 4	-	
	Reserved	Bit 5	-	
	Reserved	Bit 6	-	
	Reserved	Bit 7	-	
0x19	PlusHVOverMask	Bit 0	R/W	PlusHVOver Masking bit (default 0)
	MinHVOverMask	Bit1	R/W	MinHVOver Masking bit (default 0)
	VDROverMask	Bit 2	R/W	VDROver Masking bit (default 0)
	PlusVOPOverMask	Bit 3	R/W	PlusVOPOver Masking bit (default 0)
	MinVOPOverMask	Bit 4	R/W	MinVOPOver Masking bit (default 0)
	OverTemp_PSMask	Bit 5	R/W	OverTemp Masking bit (default 0)
	OverTemp_CoilMask	Bit 6	R/W	OverTemp2 Masking bit (default 0)
	AmpFailMask	Bit 7	R/W	AmpFail Masking bit (default 0)
0x1A	PlusHVUnderMask	Bit 0	R/W	PlusHVUnder Masking bit (default 0)
	MinHVUnderMask	Bit 1	R/W	MinHVUnder Masking bit (default 0)
	VDRUnderMask	Bit 2	R/W	VDRUnder Masking bit (default 0)
	PlusVOPUnderMask	Bit 3	R/W	PlusVOPUnder Masking bit (default 0)
	MinVOPUnderMask	Bit 4	R/W	MinVOPUnder Masking bit (default 0)
	UnderTemp_PSMask	Bit 5	R/W	UnderTemp Masking bit (default 0)
	UnderTemp_CoilMask	Bit 6	R/W	UnderTemp2 Masking bit (default 0)
	Reserved	Bit 7	-	
0x1B	DCErrorMask	Bit 0	R/W	DCError Masking bit (default 0)
	OverloadErrorMask	Bit 1	R/W	OverloadError Masking bit (default 0)
	Reserved	Bit 2	-	
	CMErrorMask	Bit 3	R/W	CMError Masking bit (default 0)
	MOSFailErrorMask	Bit 4	R/W	MOSFailError Masking bit (default 0)
	Reserved	Bit 5	-	
	Reserved	Bit 6	-	
	Reserved	Bit 7	-	
0x1C... 0x1F	Reserved	-	-	

Table 13 Register Map

4.2.2 Programmable GPIO

When configured as output, the programmable GPIO allows setting an interrupt for an external system host to read status whenever an error occurs, or when configured as input, to allow function as I2C expander to read one external logic signal via I2C.

4.2.2.1 GPIO as output

Any protection system error flag available in I2C register 0x0A-0x0D can be set to assert the GPIO output high as interrupt for a system host to read back error status. The GPIO value clears upon read back of any of these registers.

The GPIO output can be forced either high or low by I2C. This value is cleared either by setting it low, or by reading any I2C register.

Which error/status flags to trigger the GPIO can be selected by writing de-masking bits to I2C register 0x18-0x1B. Each de-masking bit is active high: Each bit set high will allow the corresponding signal to assert the GPIO signal.

Register 0x18-0x1B can be read back for current list of masking bit status.

4.2.2.2 GPIO as input

If configured as input, the logic level of the GPIO pin is monitored by the on-board uC and mapped to a dedicated I2C register (0x09, bit 1). This feature can be thought of as a "HW-logic-level to SW-register-bit" converter, i.e., the system host controller can read a physical logic-level signal via the 1ET9040BA.

For example, in case the System Controller lacks available logic-level inputs, but it is desirable to monitor the Ready signal from a PSU, the Ready signal can be physically wired to the GPIO and the System Controller can access its status via the 1ET9040BA register map.

5 Mechanical Specifications

5.1 Module Dimensions

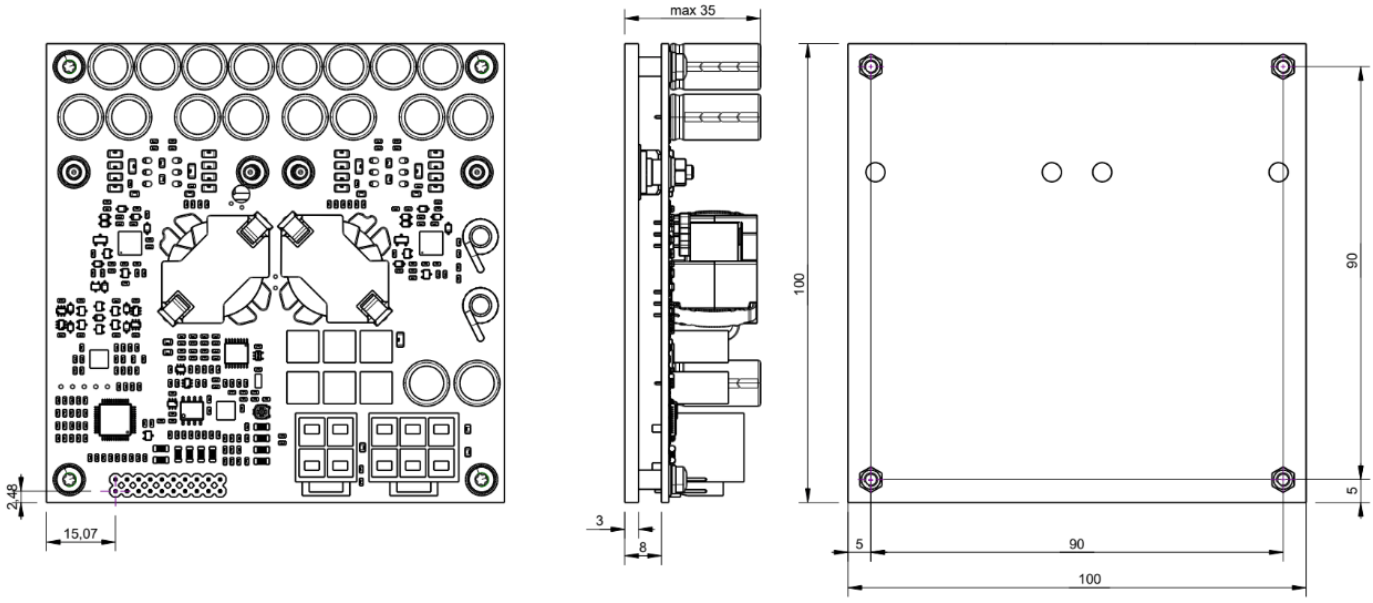


Figure 17 Dimensions

6 Compliance & Robustness Testing

1ET9040BA is designed with considerations for robustness of the end application. However, it is the responsibility of the system integrator to ensure any form of design-for-compliance and associated testing/certification which may be required.

7 Revision History

Rev	Date	Description	ID
0.90	2023-06	First pre-release version	CNN
0.91	2023-06	Height corrected	CNN

Table 14 Revision History